PROGRAMMABLE SINGLE-CHIP HIGH-SPEED PULSE GENERATOR
PCL-240K

(1) FEATURES

- •Operates on a single +5V power.
- •Plastic 40P dip
- •Directly connectable to an 8-bit microprocessor.
- •Speed can be changed even during operation.
- •Small-sized package.
- •Low price.
- •Improved reliability.
- •High accuracy.

(2) GENERAL DESCRIPTION

The PCL-240K is a CMOS LSI developed to control stepper motors and DC servomotors. It generates pulse under the condition set by the CPU.

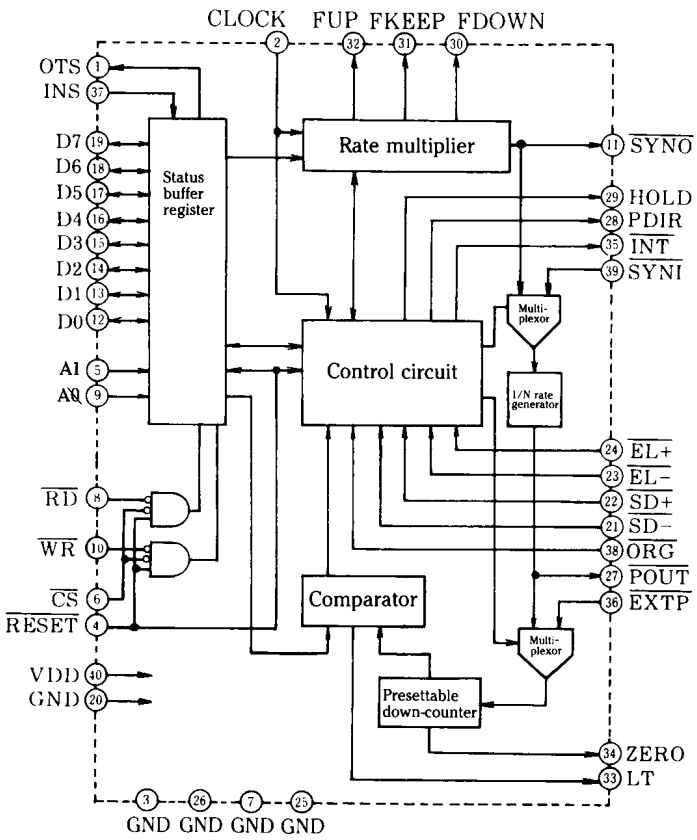
Use of multiple units of PCL-240K allows for synchronized control of multiple shafts.

A 24-bit presettable binary counter is provided.

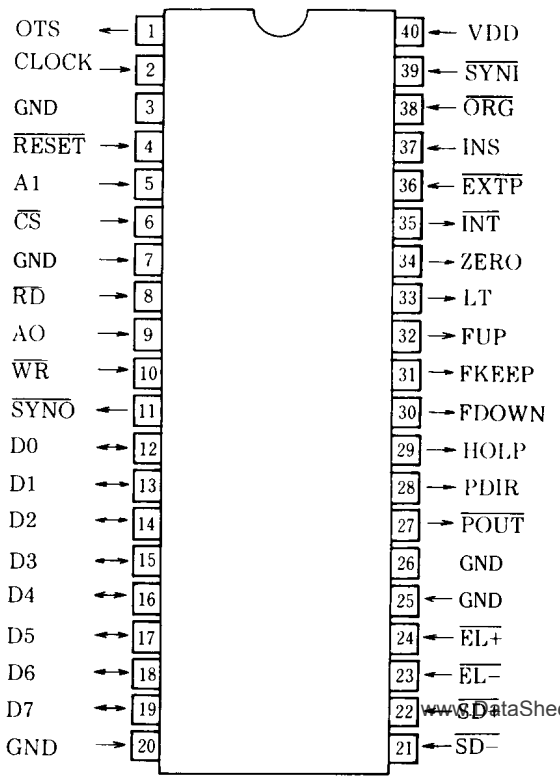
(3) APPLICATIONS

- •Numerically-controlled machine tool
- •Robot
- •Pulse generator, etc.

(4) BLOCK DIAGRAM



Pin assignment (top view)



(5) SPECIFICATIONS

(1) Power supply:	+5V ±5%
(2) Reference clock:	4.9152 MHz
(3) Number of pulses selectable:	1 to 16,777,215 pulses
(4) Frequency setting steps:	8191 steps (1 to 8191)
(5) Frequency multiplier:	1x ~ 30x 1x mode: 1 pps/step 30x mode: 30 pps/step
(6) Output frequency range:	1x mode: 1 to 8191 pps 30x mode: 30 to 245730 pps
(7) Frequency registers:	3 kinds of FL, FH1 and FH2
(8) Ramping-down point setting range:	1 to 1048575 pulses
(9) Acceleration rate setting range:	2 to 16383
(10) Deceleration rate setting range:	2 to 16383
(11) Operation modes:	•High speed consistent mode (with acceleration and deceleration •Constant speed consistent mode •High speed variable mode (with automatic acceleration and deceleration) •Constant speed variable mode •High speed origin return mode •Constant speed origin return mode •Dual rate mode (ramping up) •Dual rate mode (ramping down) •Immediate stop mode •Deceleration-stop mode
(12) Output signals:	At common pulse mode — +/− direction and clock out signals At independent pulse mode — (+) clock: outputted from $\overline{\text{POUT}}$ (−) clock: outputted from $\overline{\text{PDIR}}$

1. Electrical Characteristics

1) Maximum absolute ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.5 to +7	V
Input voltage	V_I	−0.5 to V_{DD}+0.5	V
Output current	I_O	20	mA
Storage temperature	Tstg	−65 to +150	°C

2) Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.75	5	5.25	V
Ambient temperature	Ta	0		+70	°C
Low level input voltage	V_{IL}	0		0.8	V
High level input voltage	V_{IH}	2.0		V_{DD}	V
Input rise/fall time	tr, tf	0		10	μs

3) Input/output capacity

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input terminal	C_{IN}	$V_{DD} = V_I = 0$			10	PF
Output terminal	C_{OUT}	f = 1 MHz			15	PF
Input/output terminal	$C_{I/O}$				20	PF

4) Electrical characteristics (V_{DD} = 5V ± 5%, Ta = 0 to +70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	I_{DD}	*1			5	mA
Off-state output leak current	I_{OZ}	$V_O = V_{DD}$ or GND			10	μA
Input current*2	I_{I1}	$V_I = V_{DD}$ or GND		10^{-5}	10	μA
Input current*3	I_{I2}	V_I = GND	25	80	250	μA
Low-level output current*4	I_{OL}	V_{OL} = 0.4V	4.3	11		mA
Low-level output current*5	I_{OL}	V_{OL} = 0.4V	6	15		mA
High-level output current*4	I_{OH}	$V_{OH} = V_{DD} - 0.4V$	−4.3	−8		mA
High-level output current*5	I_{OH}	$V_{OH} = V_{DD} - 0.4V$	−6	−11		mA
Low-level output voltage	V_{OL}	I_O = 0mA			0.1	V
High-level output voltage	V_{OH}	I_O = 0mA	$V_{DD} - 0.1$			V
Built-in pull-up resistor*3	R_{UP}		22	62.5	180	KΩ
Output rise time	T_{or}	C_L = 15PF		3.5		nS
Output fall time	T_{of}	C_L = 15PF		2.5		nS

*1: Reference clock 4.9152MHz, output clock 245,730 pps when unloaded.
*2: CLOCL, $\overline{\text{RESET}}$, A0 ~ 1, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, D0 ~ 7 signals
*3: $\overline{\text{SD}}$+, $\overline{\text{SD}}$−, $\overline{\text{EL}}$+, $\overline{\text{EL}}$−, $\overline{\text{EXTP}}$, INS, $\overline{\text{ORG}}$ signals
*4: D0 ~ 7
*5: OTS, $\overline{\text{POUT}}$, PDIR, HOLD, FDOWN, FKEEP, FUP, LT, ZERO, $\overline{\text{INT}}$ signals

5) AC characteristics

Clock

Item	Symbol	Condition	Min.	Max.	Unit
Clock cycle	t_{CLK}		124	(DC)	ns
Low power time	t_{PWL}		83		ns
High power time	t_{PWH}		41		ns

Read cycle

Item	Symbol	Condition	Min.	Max.	Unit
Address stabilizing time	t_{AR}		18		ns
Address holding time	t_{RA}		0		ns
Read pulse width	t_{RR}		31		ns
Data delay time	t_{RD}	C_L = 15pF		31	ns
Data float delay time	t_{DF}	C_L = 15pF	7	28	ns

Write cycle

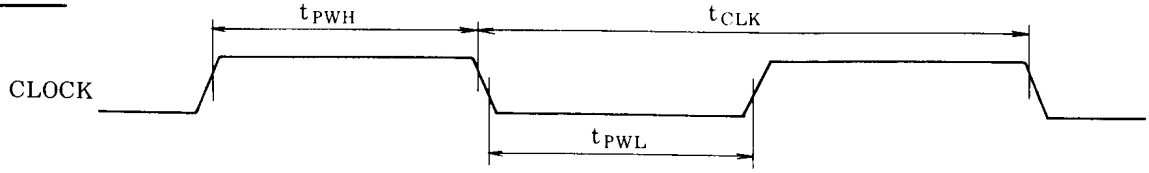
Item	Symbol	Condition	Min.	Max.	Unit
Address stabilizing time	t_{AW}		8		ns
Address holding time	t_{WA}		10		ns
Write pulse width	t_{WW}		22		ns
Data setting time	t_{DW}		15		ns
Data holding time	t_{WD}		24		ns

Reset cycle

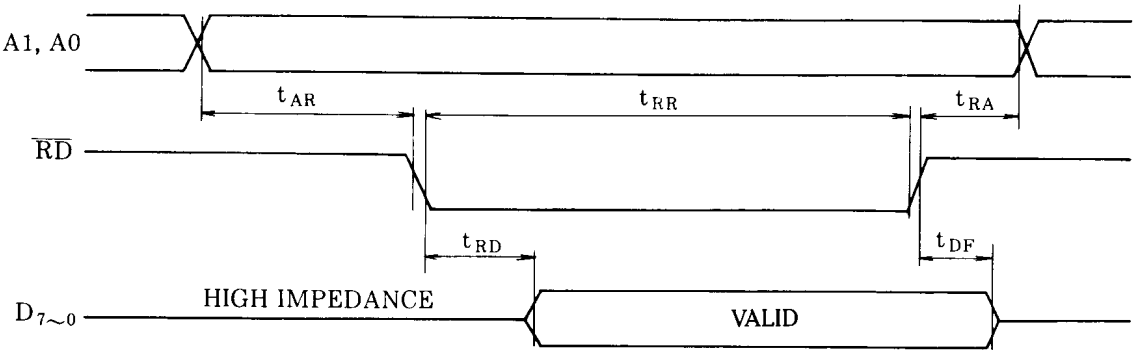
Item	Symbol	Condition	Min.	Max.	Unit
$\overline{\text{RESET}}$ pulse width	t_{RST}		$3 \cdot t_{CLK}$		ns
Resetting time	t_{RSTM}			$3 \cdot t_{CLK}$	ns

6) Timing chart

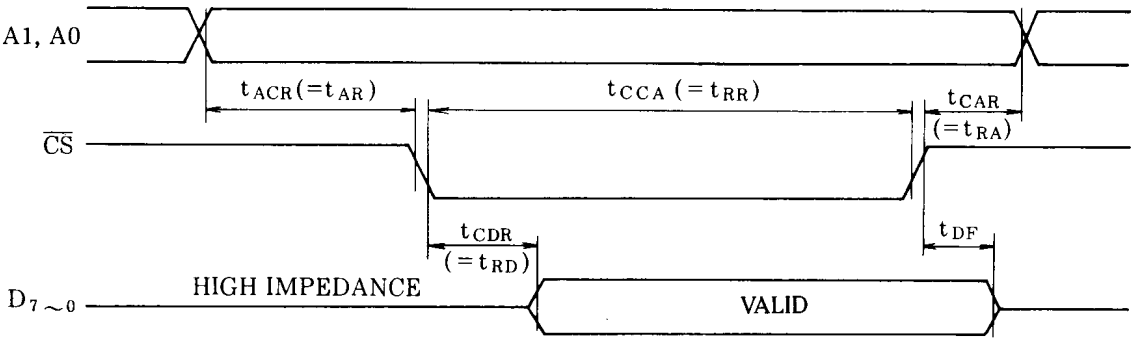
Clock



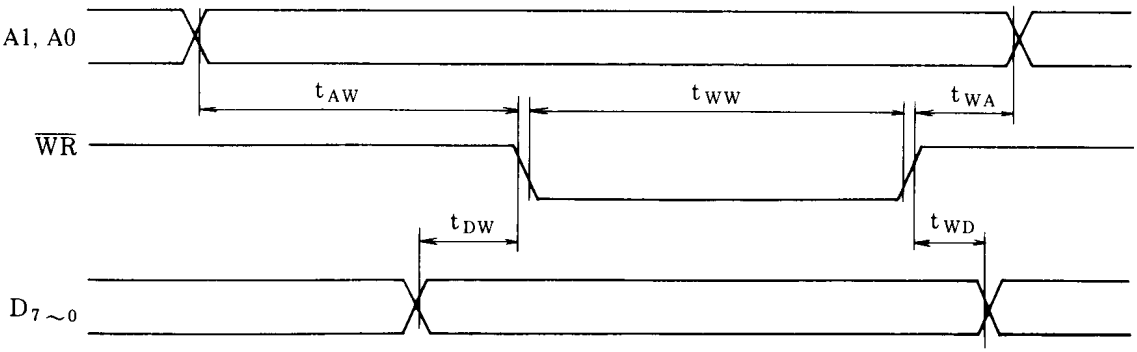
Read cycle 1 ($\overline{CS}$=V_{IL})



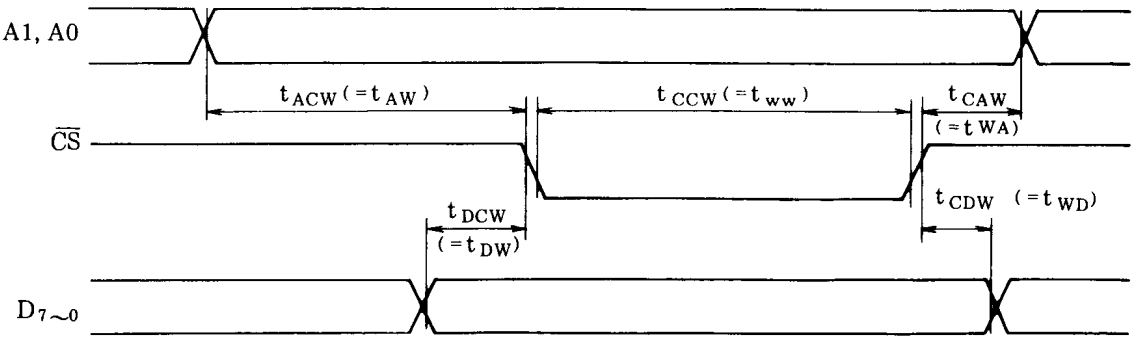
Read cycle 2 ($\overline{RD}$=V_{IL})



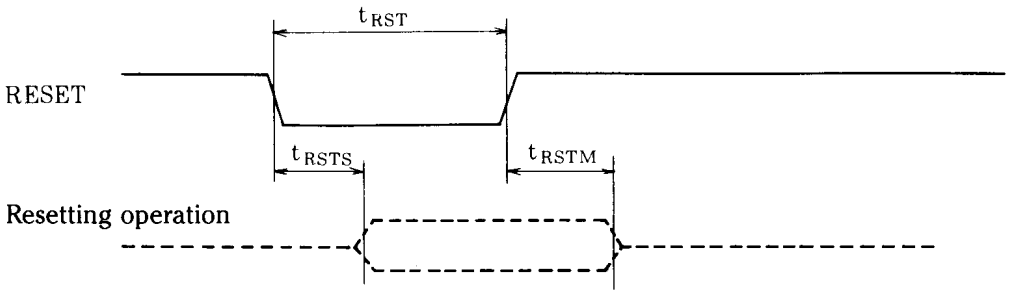
Write cycle 1 ($\overline{CS}$=V_{IL})



Write cycle 2 ($\overline{WR}$=V_{IL})



Reset cycle timing



2. Pin Functions (figures in parentheses are pin number)

(1) OTS (Output Signal) ..... Output

It is a multi-purpose output signal and can be controlled through the CPU.

(2) CLOCK (Clock) ..... Input (usually, 4.9152MHz)

It is the reference clock for the output pulse. Accuracy of the output pulse does not include that of the reference clock.

(4) $\overline{\text{RESET}}$ (Reset)..... Active low level input

It resets the internal counter and all registers when it is low level.

(5) A1, (9) A0 (Address Bus) ..... Input

They are internal register select signals and usually connected to CPU addresses 1 and 0.

(6) $\overline{\text{CS}}$ (Chip Select) ..... Active low level input

The low level signal places $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals in ENABLE condition, thereby making it possible for the CPU to read and write.

(8) $\overline{\text{RD}}$ (Read) ..... Active low level input

The low level signal lets the status or counter content be outputted to the data bus.

(10) $\overline{\text{WR}}$ (Write) ..... Active low level input

The low level signal enables the counter and register to write.

(11) $\overline{\text{SYNO}}$ (Synchro Out) ..... Active low level output

Synchronized clock is outputted for synchronized operation of multiple units of PCL-240K.

(12 to 19) D0 to D7 (Data Bus) ..... 3-state input/output

These are dual-direction data bus.

(3, 7, 20, 25, 26) GND, (40) V_{DD} ..... Power inputs

Input +5V to V_{DD} and 0V to all GNDs.

(21) $\overline{\text{SD}-}$, (22) $\overline{\text{SD}+}$ (Slow Down) ..... Active low level inputs (built-in pull-up resistor)

Effective in SD enable mode (refer to control mode)

When a signal of the same direction as that of output pulse is low level during operation in the high speed mode, the frequency ramps down.

If it is high level after then, the frequency ramps up.

(23) $\overline{\text{EL}-}$, (24) $\overline{\text{EL}+}$ (End Limit) ..... Active low level inputs (built-in pull-up resistor)

When a signal of the same direction as that of the PDIR signal is low level during pulse output, pulse output stops immediately. During the low level, pulse cannot be outputted toward the direction but can be outputted toward the opposite direction.

(27) $\overline{\text{POUT}}$ (Pulse Output) ..... Active low level output

It is the pulse output pin. Its duty cycle is approx. 50%.

(28) PDIR (Pulse Direction) ..... Output

It gives the direction signal of output pulse. When it is low level, the minus direction signal is outputted.

(29) HOLD (Hold) ..... Active high level output

It is high level when no pulse is outputted.

(30) FDOWN (Frequency Down) ..... Active high level output

It is high level while frequency ramps down during operation in the high speed mode.

(31) FKEEP (Frequency Keep) ..... Active high level output

It is high level when frequency is not ramping up nor down. It can be read in as a status signal.

(32) FUP (Frequency UP) ..... Active high level output

It is high level while frequency is ramping up during operation in the high speed mode.

(33) LT (Little) ..... Active high level output

It is high level when the counter content is smaller than the down-point register value.

(34) ZERO (Zero) ..... Active high level output

It is high level when the counter content is 0.

(35) $\overline{INT}$ (Interrupt Request) ..... Active low level output

It is low level when the output pulse stops.

It can be masked by CPU command.

It can be read as a status signal.

(36) $\overline{EXTP}$ (External Pulse) ..... Active low level input

When operating the counter through an external pulse, input the pulse to this pin. The counter counts the pulse at the edge of rise.

(37) INS (Input Signal) ..... Input (built-in pull-up resistor)

It is a multi-purpose input and the CPU can read the signal as a status signal.

(38) $\overline{ORG}$ (Origin) ..... Active low level input (built-in pull-up resistor)

When it is low level during return to the mechanical origin, pulse output stops immediately. The signal can be read as a status signal.

(39) $\overline{SYNI}$ (Synchro In) ..... Active low level input

For synchronized operation, it inputs the synchronized clock.

3. Basic Functions

$\overline{CS}$	A1	A0	$\overline{RD}$	$\overline{WR}$	
0	0	0	1	0	Data bus to command buffer
0	0	1	1	0	Data bus to register bits 0 to 7
0	1	0	1	0	Data bus to register bits 8 to 15
0	1	1	1	0	Data bus to register bits 16 to 23
0	0	0	0	1	Data bus from status
0	0	1	0	1	Data bus from counter output bits 0 to 7
0	1	0	0	1	Data bus from counter output bits 8 to 15
0	1	1	0	1	Data bus from counter output bits 16 to 23
1	×	×	×	×	D0 ~ D7 = high impedance
0	×	×	0	0	Inhibit

1) Command buffer

The PCL-240 has various functions to drive and control stepper motors and DC servomotors. The command buffer is provided to select functions. Once a command is set, it is not changed until a new command is entered. For the starting mode only, the command reset is provided.

D7	D6	D5	D4	D3	D2	D1	D0
C1	C0						

C — Command

C1	C0	
0	0	Operating mode selection
0	1	Control mode selection
1	0	Data register selection
1	1	Output pulse mode selection

a) Operating mode selection

7	6	5	4	3	2	1	0
0	0						

- Frequency selection
- 0 : Constant speed mode
  1 : High speed mode
- 1 : Start/stop control
- 0 : INT F/F reset
  1 : Cancellation of INT F/F reset

0	0	*	1	0	0	0	0	Constant speed operation with the FL register

Operates at the speed set for the FL register.

0	0	*	1	0	0	0	1	Constant speed operation with the FH1 register

Operates at the speed set for the FH1 register.

0	0	*	1	0	0	1	1	Constant speed operation with the FH2 register

Operates at the speed set for the FH2 register.

0	0	*	1	0	1	0	1	High speed dual rate operation with the FH1 (ramping up halfway)

Frequency ramps up halfway from the rate of the FL to that of the FH1.

0	0	*	1	0	1	1	1	High speed dual rate operation with the FH2 (ramping up halfway)

Frequency ramps up halfway from the rate of the FL to that of the FH2.

0	0	*	1	0	1	0	0	Dual rate operation (ramping down)

Frequency ramps down to the rate of the FL.

0	0	*	1	1	1	1	1	Decelerating stop (reset command is required after stop)

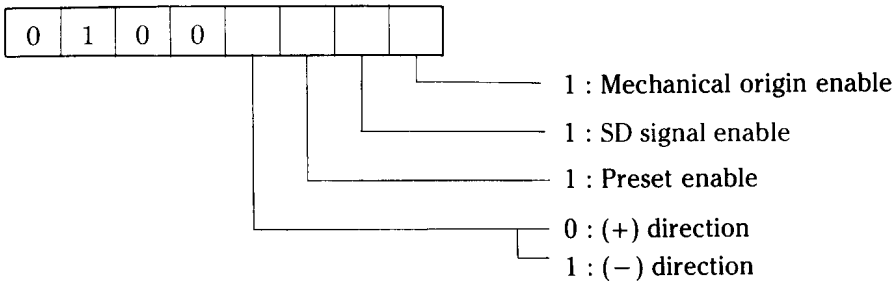
Frequency ramps down to the speed set for the FL, then pulse stops.

0	0	0	0	1	0	0	0	Reset command

This stops pulse generation under any condition. If you start with the start command, be sure to reset with the reset command before the next start.

Note: * 0 (no output of $\overline{INT}$ signal at stop)
1 (output of $\overline{INT}$ signal at stop)

b) Control mode selection



Examples

0	1	0	0	*	0	0	0

Manual mode

Operation initiated in the start mode continues until the stop command is transferred.

0	1	0	0	*	0	0	1

Mechanical origin return mode

Operation initiated in the start mode continues until the mechanical origin signal or stop command comes.

0	1	0	0	*	1	0	0

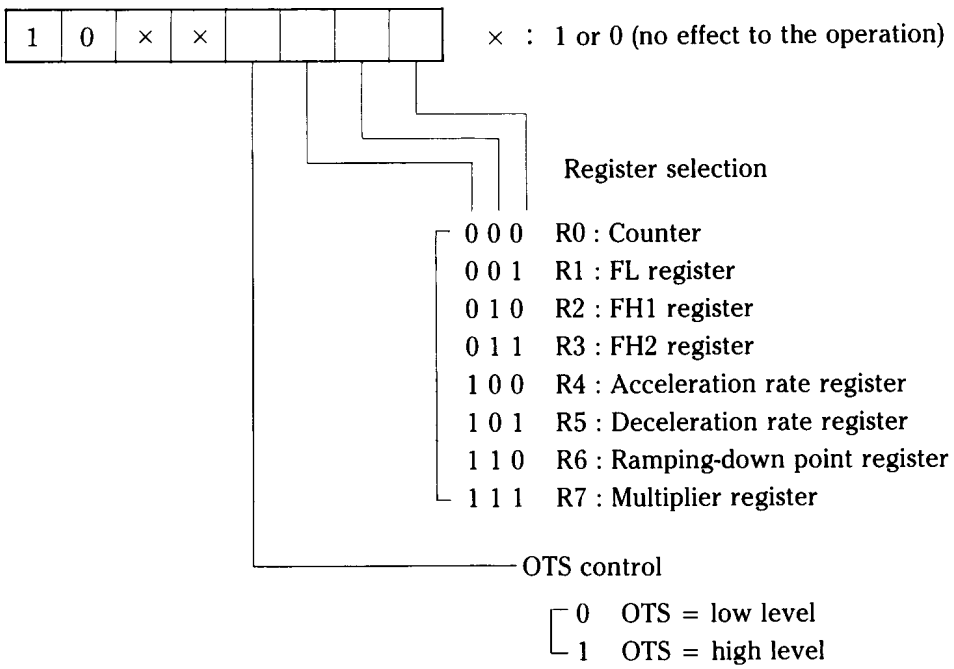
Preset mode (Preset ramping-down mode)

Operation in the constant speed start mode, stops when the quantity set for register R0 is reached.

Operation in the high speed start mode, ramps down when the quantity set for register R6 is reached and stops when the quantity set for register R0 is reached.

Note: *: 0 — (+) direction
1 — (−) direction

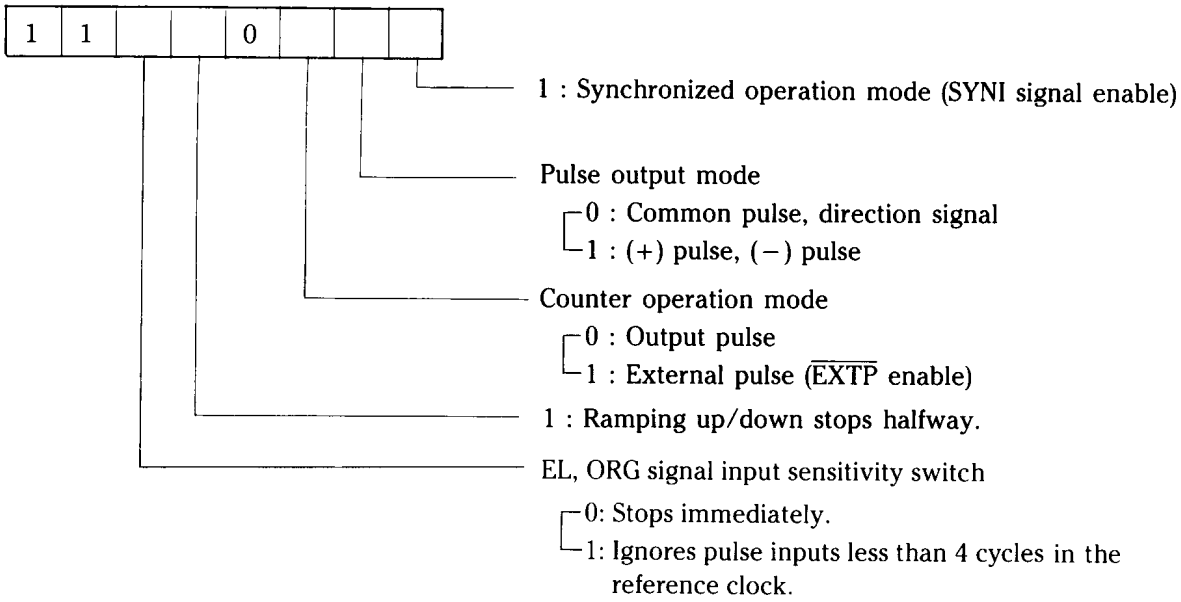
c) Register selection



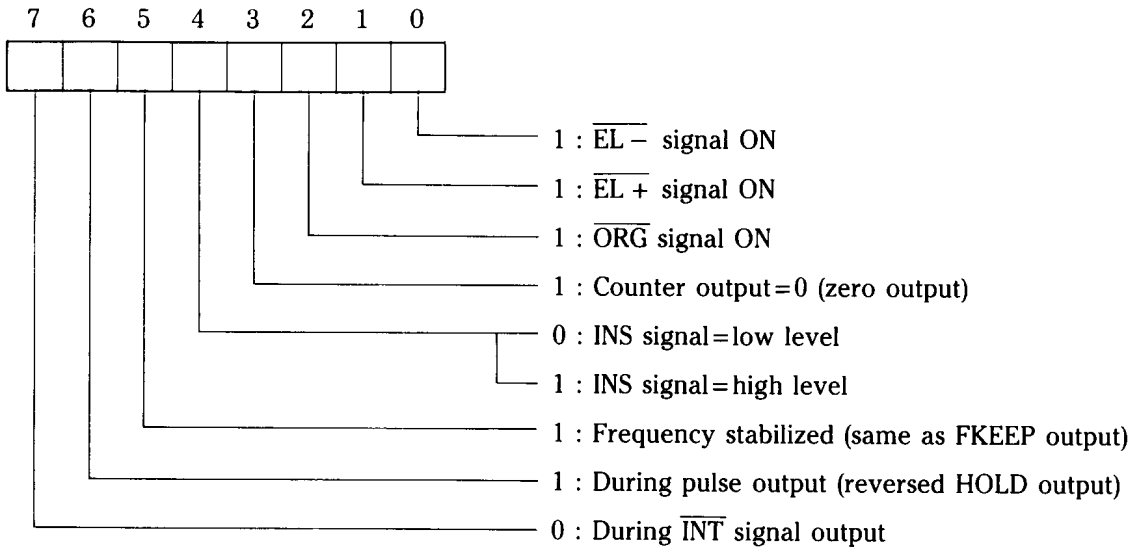
Kinds of registers and data bits

Description		Bits	Read/write
R0	Counter	24	R/W
R1	FL register	13	W
R2	FH1 register	13	W
R3	FH2 register	13	W
R4	Acceleration rate register	14	W
R5	Deceleration rate register	14	W
R6	Ramping-down point register	20	W
R7	Multiplier register	10	W

d) Output mode selection



Status



4. Functions of Built-in Registers

R0: Down-Counter (24 bits)

The down-counter counts down once at the time one pulse is outputted in any of following modes: manual mode, origin return mode and preset mode. If the counter operating mode is effective to external pulses, the counter counts down each time one pulse is inputted through the $\overline{\text{EXTP}}$ terminal.

If a pulse is outputted (or inputted) when the counter has counted down to 0, the maximum number (FFFFFF in hexadecimal notation, 16777215 in decimal notation) returns.

The counter value (number of residual pulses) can be read out during operation or standstill. When checking the value during operation, however, you need to read out twice instantly before the next pulse comes. And if the same value is readout, it indicates the true number of residual pulses.

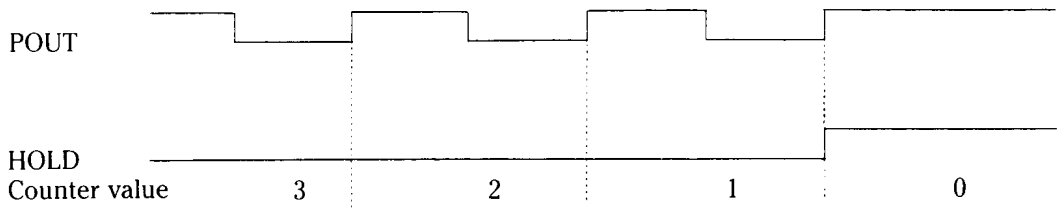
In preset mode, set the number of output pulses on this counter. The number will be counted down according to operation and pulse generation will stop at 0.

The number can be selected in a range of 000001 (hex.) to FFFFFF (hex.) which corresponds to 1 to 16777215 in decimal notation.

If the start command is inputted when the initial setting is 0, no pulse is outputted and while the operating status flag and the HOLD signal at the output terminal indicate the halt condition, the $\overline{\text{INT}}$ signal is not be outputted.

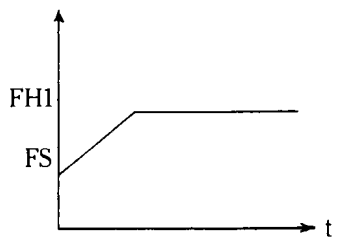
In case of the interruption by deceleration-stop command or reset command during operation, residual pulses are kept and can be outputted by only inputting the start command again.

However, you need to set a number of output pulses for every initial operation since the counter is at 0 when completed.

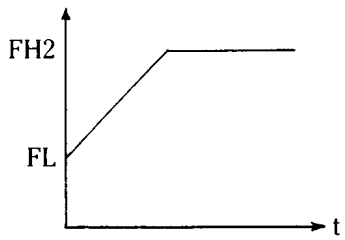


R1: FL Register (13 bits)

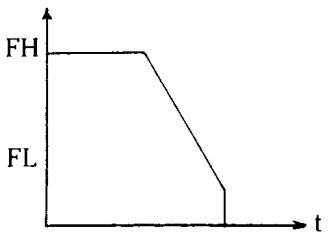
Register for setting FL speed. When started in high-speed mode, the generator starts with FL speed and then ramps up to reach the high speed. If deceleration-stop command is inputted during the high-speed operation, it ramps down then stops at FL speed. Be sure to set an FL speed.



▲ FH1 High speed start



▲ FH2 High speed start



▲ Deceleration-stop input

The setting range is 0001 (hex.) to 1FFF (hex.) which correspond to 1 to 8191 in decimal notation. Relation between a set value and the output pulse frequency varies according to the value set on the R7 (multiplier register).

R2: FH1 Register (13 bits)

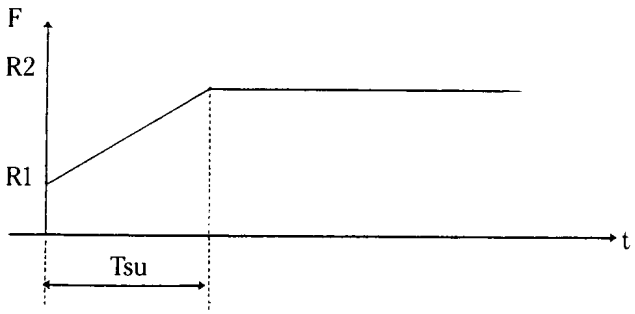
Register for setting FH1 speed. The setting range is 0001 (hex.) to 1FFF (hex.) which correspond to 1 to 8191 in decimal notation. Relation between a set value and the output pulse frequency varies according to the value set on the R7 (multiplier register).

R3: FH2 Register (13 bits)

Register for setting FH2 speed. The setting range is 0001 (hex.) to 1FFF (hex.) which correspond to 1 to 8191 in decimal notation Relation between a set value and the output pulse frequency varies according to the value set on the R7 (multiplier register).

R4: Acceleration (Ramping-up) Rate Register (14 bits)

Register for setting the acceleration (ramping-up) characteristics. When started in high-speed mode, the generator starts with the speed set on R1 (FL-register) then accelerates to reach the FH speed set on R2 or R3 register.



When the values set on R1, R2 and R4 are (R1), (R2) and (R4), and the reference clock frequency is (T_{CLK})[sec], Tsu (the time required for ramping-up) is

$$Tsu=[(R2) - (R1)] \times (R4) \times (T_{CLK})[sec]$$

The setting range is 002 (hex.) to 3FFF (hex.) which correspond to 2 to 16383 in decimal notation.

R5: Deceleration Rate Register (14 bits)

Register for setting deceleration (ramping-down) characteristics. If $\overline{SD+}$, $\overline{SD-}$ or other speed change command, which causes deceleration, are inputted in high-speed mode, it ramps down.

Tsd (the time required for ramping-down) is

$$Tsd=[(R2) - (R1)] \times (R5) \times (T_{CLK})[sec]$$

The setting range is 002 (hex.) to 3FFF (hex.) which correspond to 2 to 16383 in decimal notation.

R6: Ramping-down Point Register (20 bits)

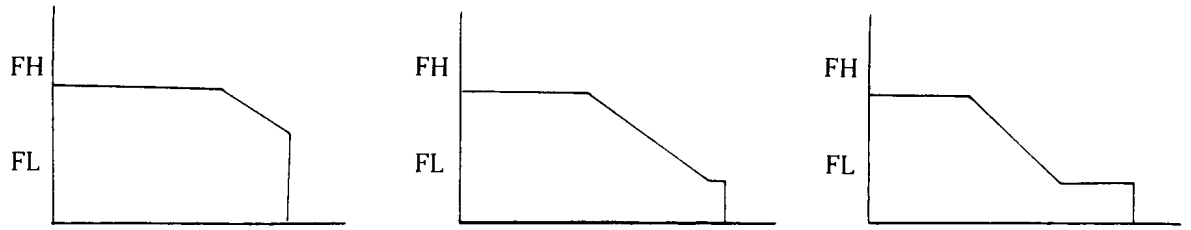
In preset high-speed operation, the value set on this register (R6) is compared with that on the down counter (R0) and the ramping-down will start when the former is larger than the latter.

If R6 > R0 before starting in preset high-speed mode, ramping-up will not occur and FL speed will be effective.

The setting range is 00001 (hex.) to FFFFF (hex.) which correspond to 1 to 1048575 in decimal notation. The ramping-down point is set based on number of pulses.

***Setting of ramping-down point**

A ramping-down point should be determined taking FL frequency, FH frequency and the deceleration rate into account. If an improper value is set, pulse output may be terminated halfway during ramping-down (Fig. A) or may continue after ramping down, causing longer FL speed operation (Fig. C).

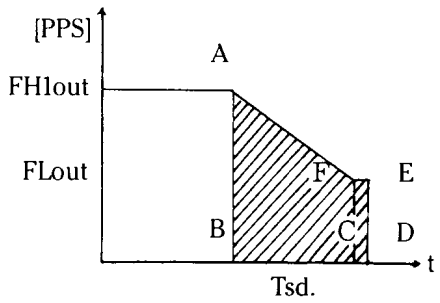


R6 setting value is too small. A

R6 setting value is optimum. (Several pulses are output at FL) B

R6 setting value is too large. C

A ramping-down point is set based on the number of pulses outputted during ramping-down. Therefore, the area marked by oblique lines in the chart at right is supposed to be the number of the pulses if FLout and FHlout are output pulse frequencies.



Tstep [sec], the time required when the output frequency changes by 1 step, is

$$\text{Tstep} = \frac{\text{(Set value on deceleration rate register)}}{\text{(Reference frequency)}}$$

$$= (R5)/(CLOCK) \quad (1)$$

S, the number of steps required for the deceleration, is

$$S = \text{(Set value on FH register)} - \text{(Set value on FL register)}$$

$$= (R2) - (R1) \quad (2)$$

Tsd [sec], the time required for the deceleration is

$$Tsd = Tstep \times S$$

$$= [(R2) - (R1)] \times (R5)/(CLOCK) \quad (3)$$

Relation between set value on speed register (Rf) and output frequency (Fout [pps]) is

$$Fout = (Rf) \times (CLOCK)/[8192 \times (R7)] \quad (4)$$

Therefore, FL output frequency FLout [pps] and FH1 output frequency FHlout [pps] are

$$FLout = (R1) \times (CLOCK)/[8192 \times (R7)] \quad (5)$$

$$FHlout = (R2) \times (CLOCK)/[8192 \times (R7)] \quad (6)$$

Thus, Psd, the number of pulses outputted during Tsd [sec] is represented by the area of the trapezoid A-B-C-D.

$$Psd = [(FLout) + (FHlout)] \times Tsd/2$$

$$= [[(R1) + (R2)] \times (CLOCK)/[(8192 \times (R7)]] \times [[(R2) - (R1)] \times (R5)/(CLOCK)]/2$$

$$= [(R2)^2 - (R1)^2] \times (R5)/[16384 \times (R7)]$$

When outputting 5 pulses at FL speed after the completion of ramping-down, the set value on the ramping-down point register (R6) is

$$(R6) = Psd + 5$$

$$(R6) = \frac{[(R2)^2 - (R1)^2] \times (R5)}{16384 \times (R7)} + 5$$

In the same manner, in case of ramping-down from FH2 speed, (R6) is

$$(R6) = \frac{[(R3)^2 - (R1)^2] \times (R5)}{16384 \times (R7)} + 5$$

R7: Multiplier Register (10 bits)

For the speed registers (R1, R2, R3), a number of steps can be selected from a range of 1 to 8191. This register permits you to set an output frequency for the one step.

The reference clock inputted through the CLOCK terminal is divided and multiplied by the variable frequency divider and the frequency multiplier then outputted to $\overline{POUT}$ terminal. When a set value on speed register is (Rf), frequency Fpout [pps] of the clock outputted from the $\overline{POUT}$ terminal is

$$Fpout = \frac{(\text{Reference clock frequency [Hz]}) \times (Rf)}{8192 \times (R7)}$$

$$= (Rf) \times \frac{(\text{Reference clock frequency [Hz]})}{8192 \times (R7)}$$

When (reference clock)/[8192 x (R7)] = 1 ..... 1x mode
When (reference clock)/[8192 x (R7)] = 10 ..... 10x mode
When (reference clock)/[8192 x (R7)] = 30 ..... 30x mode

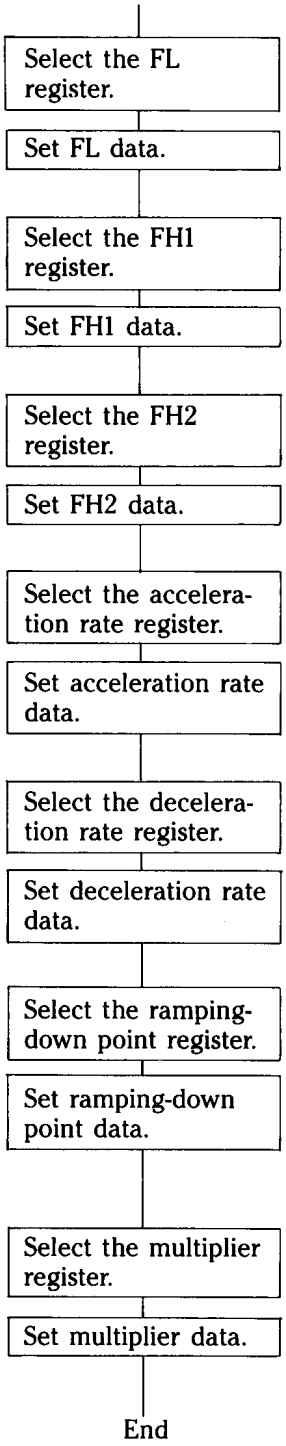
If the reference clock frequency is 4.9152 [MHz],

(R7) = 600	(= 258 [hex.])	1 x mode
(R7) = 60	(= 03C [hex.])	10x mode
(R7) = 20	(= 014 [hex.])	30 x mode

The setting range is 002 [hex.] to 3FF [hex.] which correspond to 2 to 1023 in decimal notation.
The smaller the set value, the higher the output clock frequency.

5. Typical Operation Procedure

a) Setting speed data



Command buffer ← 10000001 (81H)

Register bits 0 to 7 ← FL data, low-place 8 bits
Register bits 8 to 15 ← FL data, high-place 5 bits

Command buffer ← 10000010 (82H)

Register bits 0 to 7 ← FH1 data, low-place 8 bits
Register bits 8 to 15 ← FH1 data, high-place 5 bits

Command buffer ← 10000011 (83H)

Register bits 0 to 7 ← FH2 data, low-place 8 bits
Register bits 8 to 15 ← FH2 data, high-place 5 bits

Command buffer ← 10000100 (84H)

Register bits 0 to 7 ← Acceleration rate data, low-place 8 bits
Register bits 8 to 15 ← Acceleration rate data, high-place 6 bits

Command buffer ← 10000101 (85H)

Register bits 0 to 7 ← Deceleration rate data, low-place 8 bits
Register bits 8 to 15 ← Deceleration rate data, high-place 6 bits

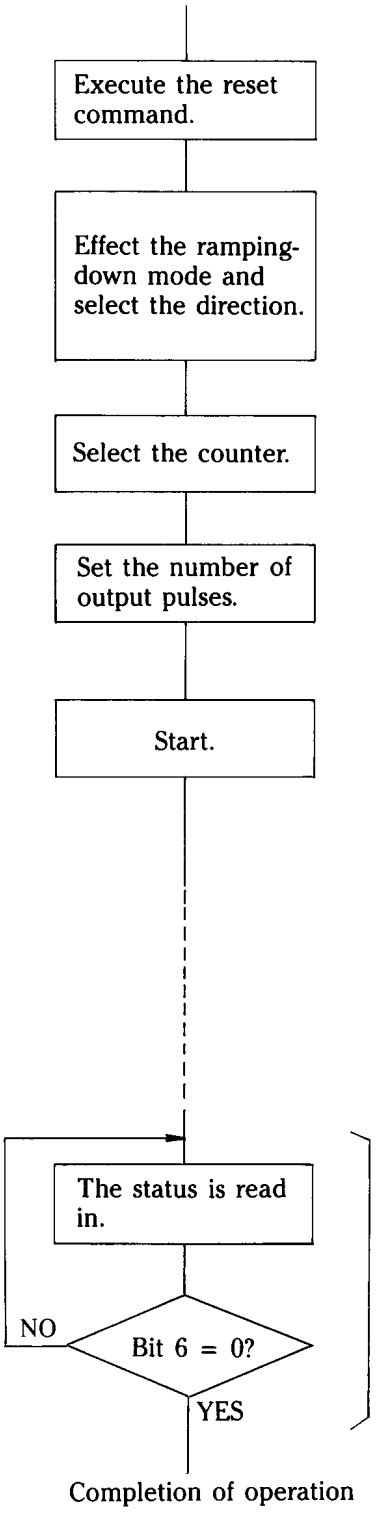
Command buffer ← 10000110 (86H)

Register bits 0 to 7 ← Ramping-down point data, low-place 8 bits
Register bits 8 to 15 ← Ramping-down point data mid-place 8 bits
Register bits 16 to 23 ← Ramping-down point data, high-place 4 bits

Command buffer ← 10000111 (87H)

Register bits 0 to 7 ← Multiplier data, low-place 8 bits
Register bits 8 to 15 ← Multiplifier data, high-place 2 bits

b) High speed preset mode



Command buffer ← 00001000 (08H)

For (+) direction
Command buffer ← 01000100 (44H)
For (−) direction
Command buffer ← 01001100 (4CH)

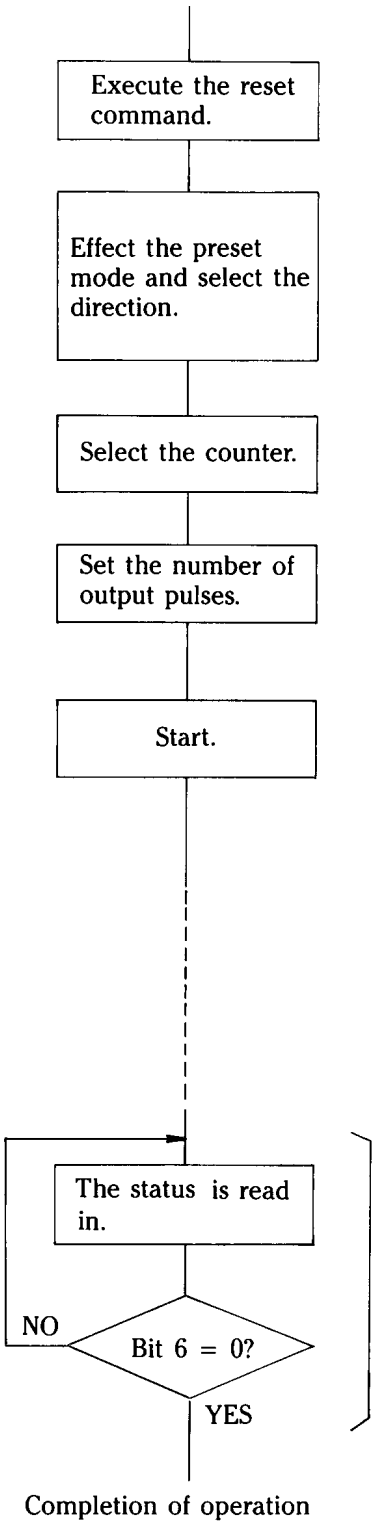
Command buffer ← 10000000 (80H)

Register bits 0 to 7 ← Data, low-place 8 bits
Register bits 8 to 15 ← Data, mid-place 8 bits
Register bits 16 to 23 ← Data, high-place 8 bits

For FH1
Command buffer ← 00010101 (15H)
For FH2
Command buffer ← 00010111 (17H)

Waiting for completion of operation.

c) Constant speed preset mode



Command buffer ← 00001000 (08H)

For (+) direction
  Command buffer ← 01000100 (44H)
For (−) direction
  Command buffer ← 01001100 (4CH)

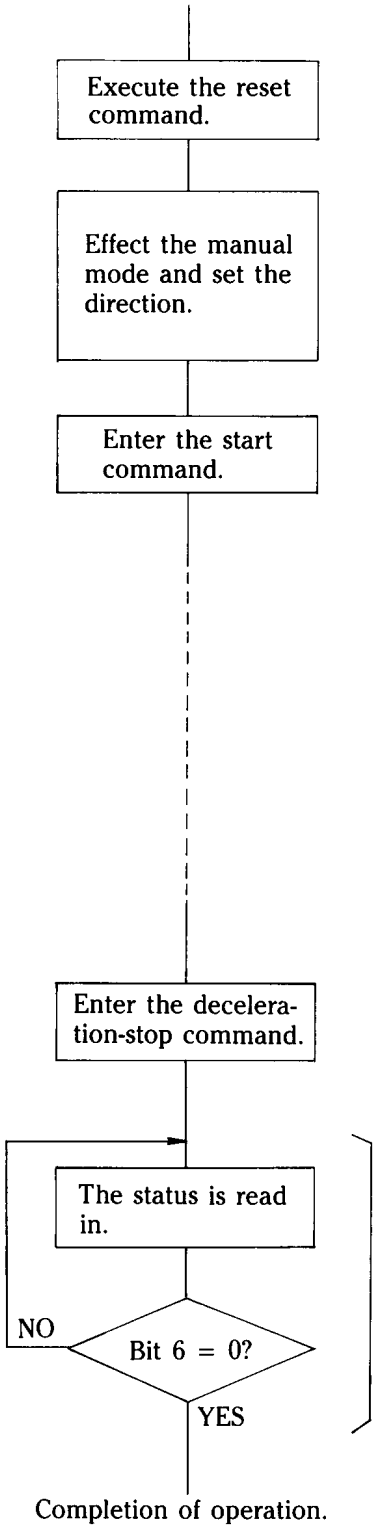
Command buffer ← 10000000 (80H)

Register bits 0 to 7 ← Data, low-place 8 bits
Register bits 8 to 15 ← Data, mid-place 8 bits
Register bits 16 to 23 ← Data, high-place 8 bits

For FL
  Command buffer ← 00010000 (10H)
For FH1
  Command buffer ← 00010001 (11H)
For FH2
  Command buffer ← 00010011 (13H)

Waiting for completion of operation.

d) High speed continuous mode



Command buffer ← 00001000 (08H)

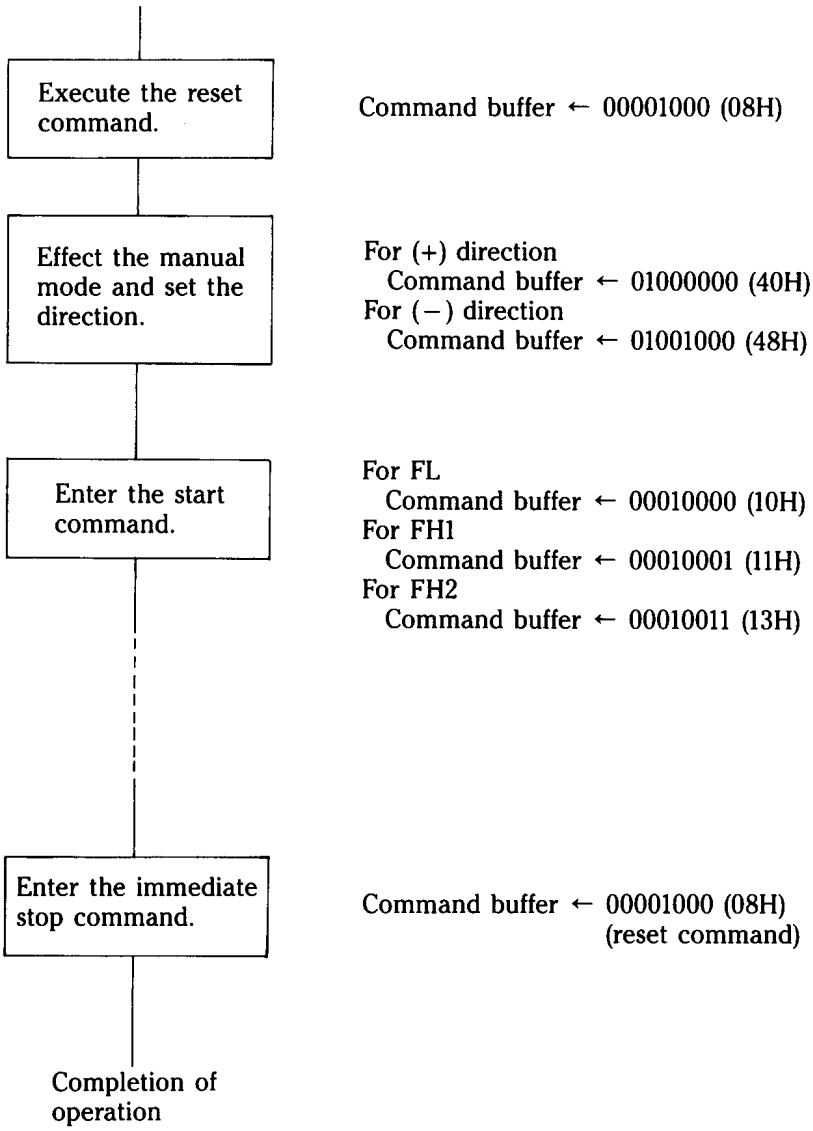
For (+) direction
Command buffer ← 01000000 (40H)
For (−) direction
Command buffer ← 01001000 (48H)

For FH1
Command buffer ← 00010101 (15H)
For FH2
Command buffer ← 00010111 (17H)

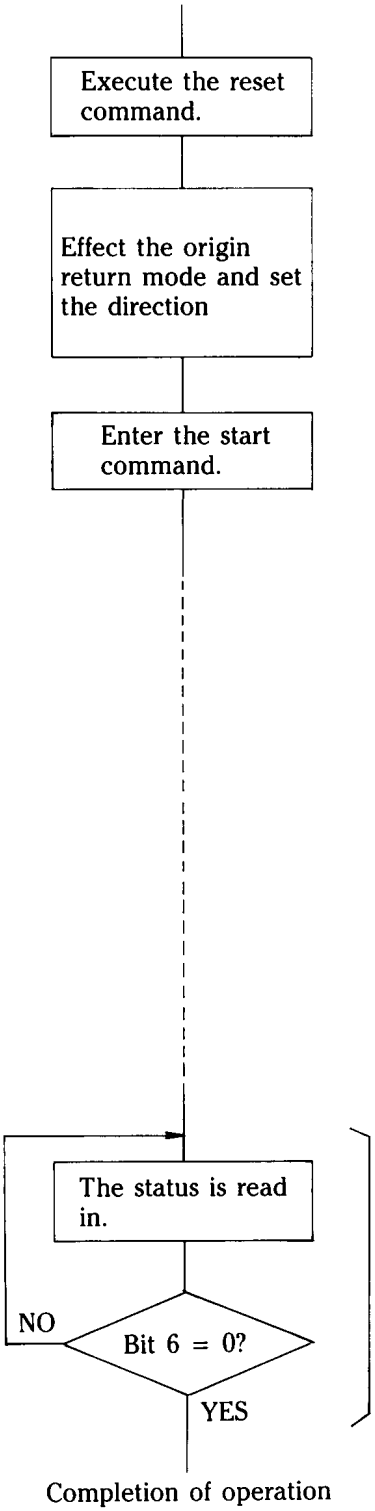
Command buffer ← 00011111 (1FH)

Waiting for deceleration-stop.

e) Constant speed continuous mode



f) High speed origin return mode



Command buffer ← 00001000 (08H)

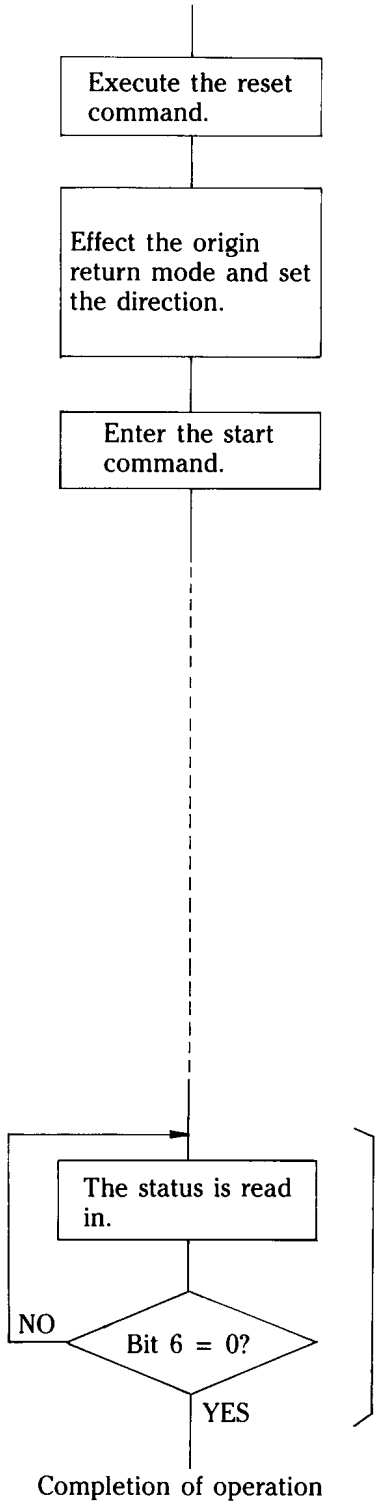
For (+) direction
Command buffer ← 01000011 (43H)
For (−) direction
Command buffer ← 01001011 (4BH)

For FH1
Command buffer ← 00010101 (15H)
For FH2
Command buffer ← 00010111 (17H)

When the $\overline{SD}$ signal of the same direction as the preset direction is low level (ON), the frequency ramps down to the rate of FL.

When the $\overline{ORG}$ signal is low level (ON), pulse output stops and status bit 6 is 0.

g) Constant speed origin return mode



Command buffer ← 00001000 (08H)

For (+) direction
  Command buffer ← 01000001 (41H)
For (−) direction
  Command buffer ← 01001001 (49H)

For FL
  Command buffer ← 00010000 (10H)
For FH1
  Command buffer ← 00010001 (11H)
For FH2
  Command buffer ← 00010011 (13H)

When the $\overline{\text{ORG}}$ signal is low level (ON), pulse output stops and status bit 6 is 0.

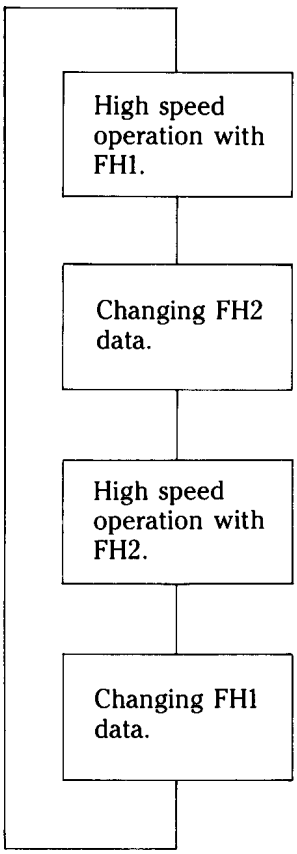
h) Speed change during operation

The PCL-240K allows for speed change during operation.

Three speed registers FL, FH1 and FH2 are provided. By entering the select command, you can let the pulse output ramp up or down to a different rate.

Further, changing the rate for the high speed register FH1 or FH2 which is not selected at the stage gives no influence to operation so you can change the rate in unlimited steps.

Example



Command buffer ← 00010101 (15H)

Command buffer ← 00010111 (17H)

Note: If the start command is entered without executing the reset command after starting, rate is changed.
To let the pulse output ramp up or down to another rate after starting in the constant speed mode, change bit 2 of the start command from 0 to 1 and enter the command before changing the rate.

6. Operation Patterns

High speed preset mode

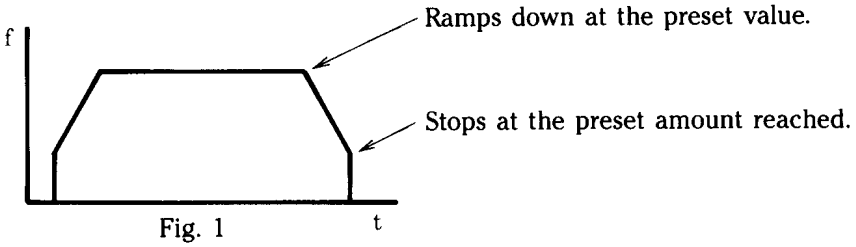


Fig. 1

Constant speed preset mode

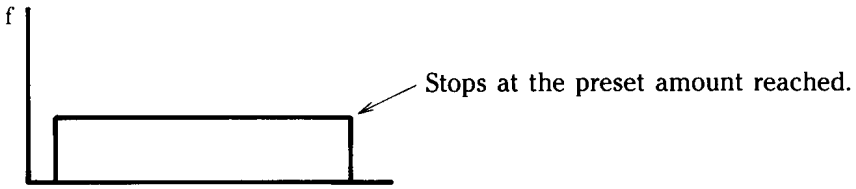


Fig. 2

High speed continuous mode

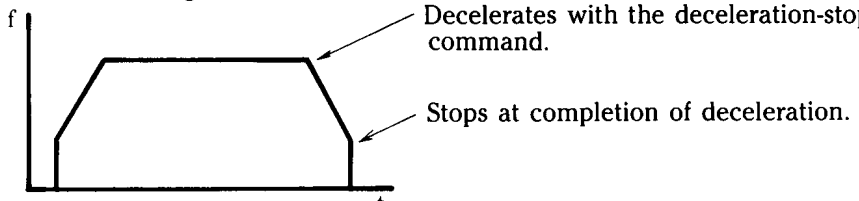


Fig. 3

Constant speed continuous mode

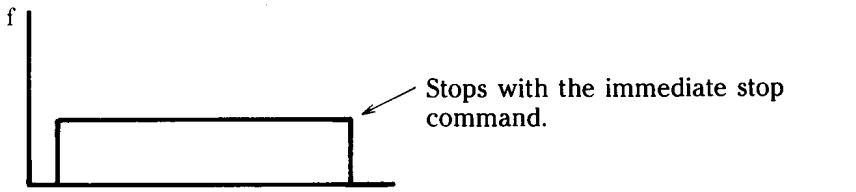


Fig. 4

High speed origin return mode

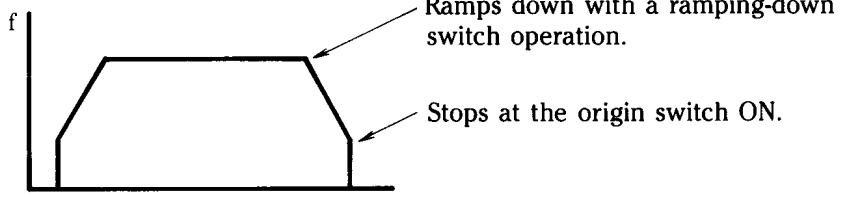


Fig. 5

Constant speed origin return mode

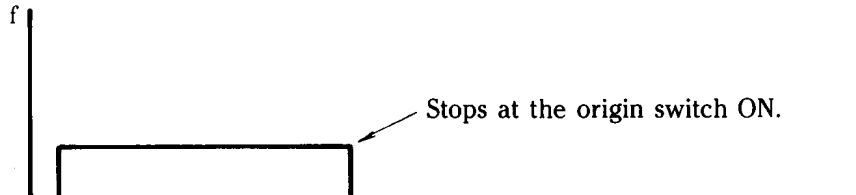


Fig. 6

Dual rate mode (1)

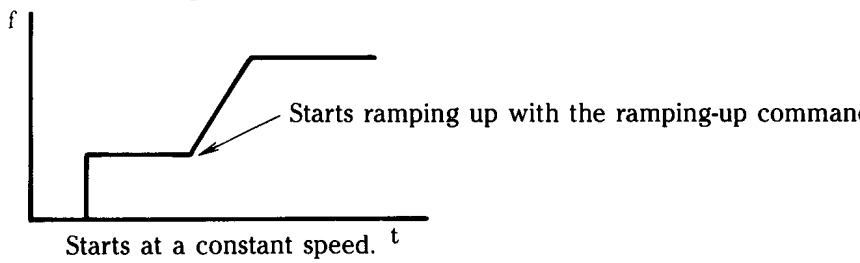


Fig. 7

Dual rate mode (2)

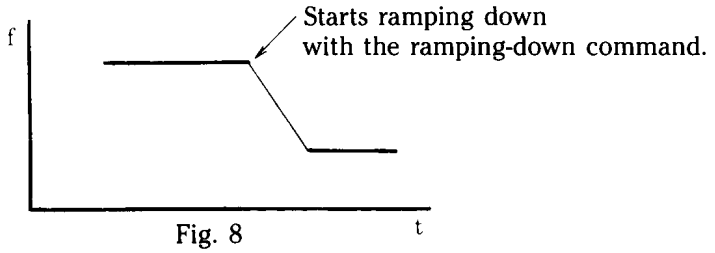
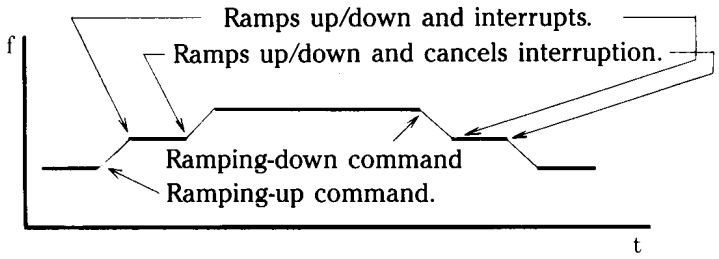
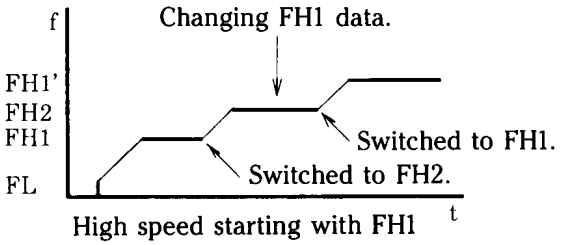


Fig. 8

Ramping up/down & interrupting mode

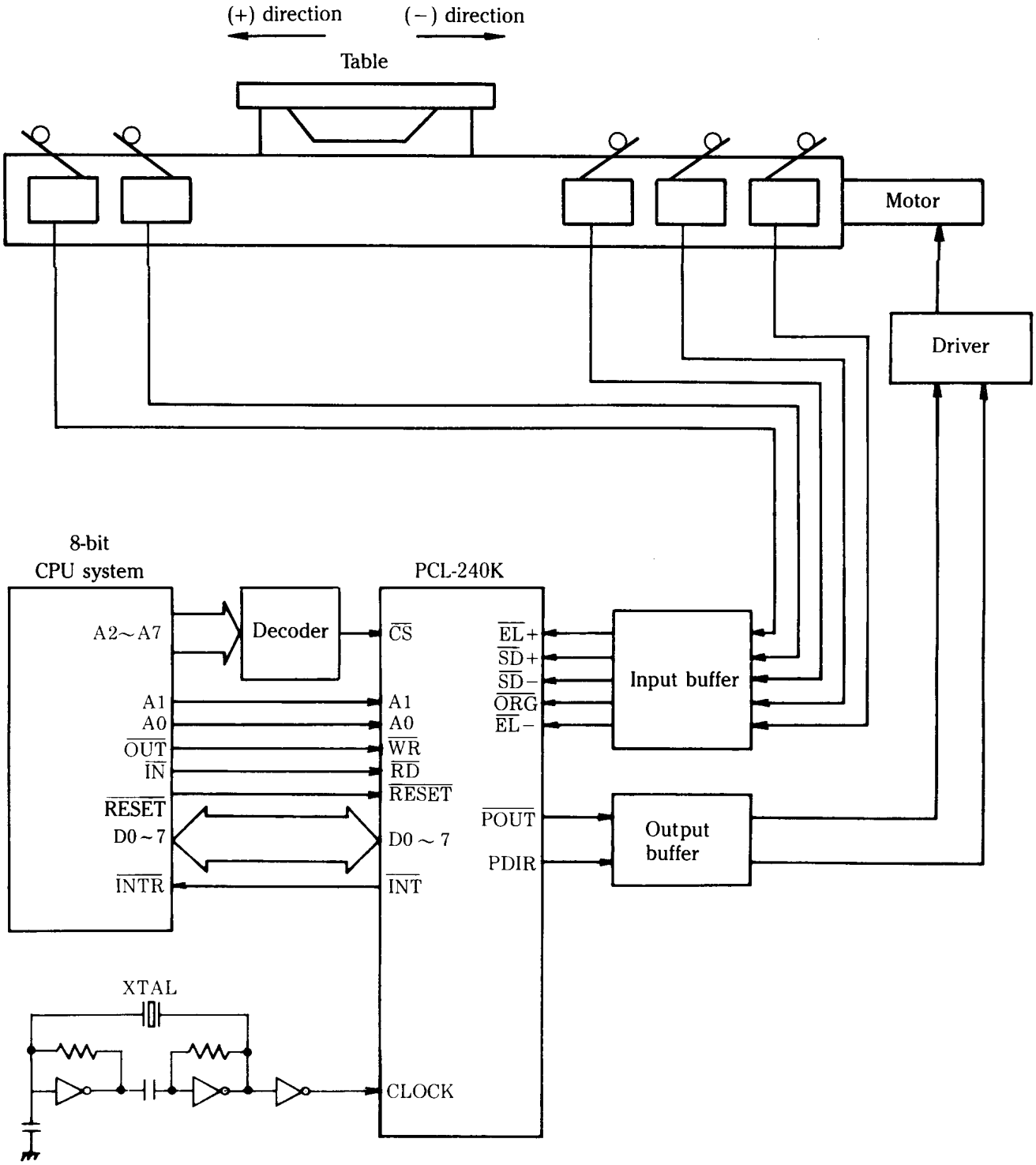


Switchover of frequency register



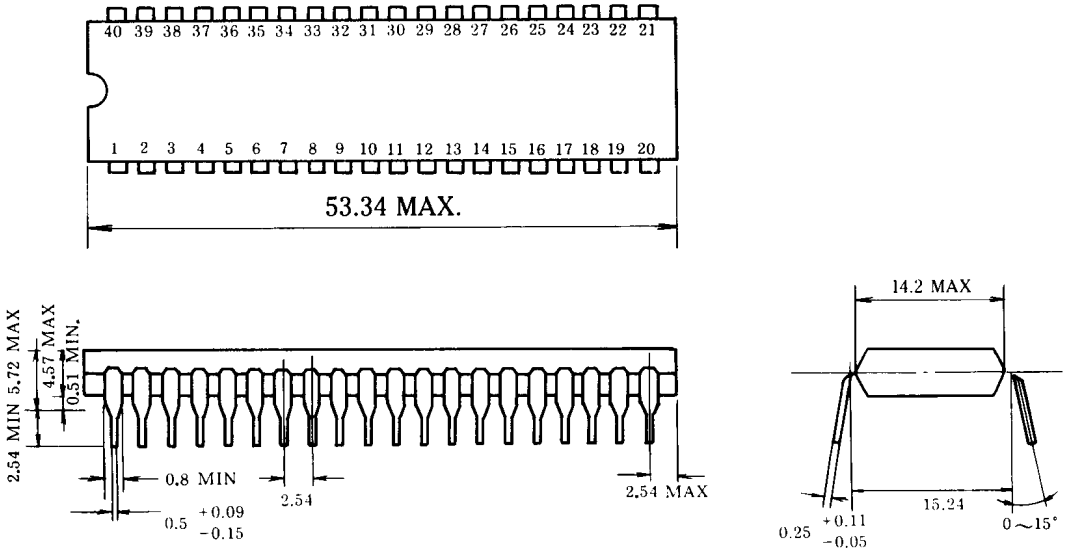
High speed starting with FH1

7. Typical System Composition



8. External Dimensions

40 Pin Plastic DIP (600 mil)



Unit: mm

PCL-240K Q & A

Q: Because a conventional IC, PCL-80K can output 80Kpps at maximum, I can guess that this new PCL-240K can output up to 240Kpps.
What's the basic difference between them?

A: The origin of this product name is just as you mentioned. In fact, the IC in the PCL-80K was capable of outputting up to max. 240K, but we restricted it to 80Kpps because we feared that there might be some claims regarding an insufficient ramping-up time or too small down-point settings if we had announced it officially at that time.
Now, we have improved this point and increased the accelerating rate by 2 bits to 14 bits and the down-point register by 7 bits to 20 bits. The PCL-240K differs from the PCL-80K basically in these two points. Other features are practically the same.

Q: However, the PCL-240K has not $\overline{\text{SYNO}}$ and $\overline{\text{SYNI}}$.

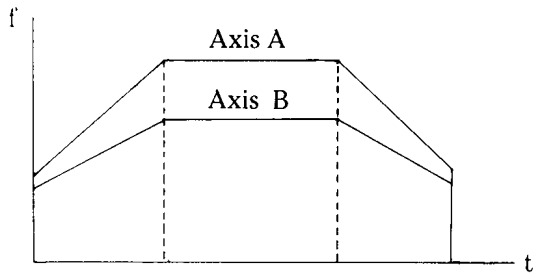
A: As you say, it might be a major difference. Though it had $\overline{\text{SYNO}}$ and $\overline{\text{SYNI}}$ to permit synchronization, their applicable name was very limited because the multiplying register had only 10 bits and many customers found out that they were practically not useful. Customers who have used $\overline{\text{SYNO}}$ and $\overline{\text{SYNI}}$ in the PCL-80K will be able to use them unchanged.

Q: Synchronous operation is not possible with the PCL-240K?

A: Yes, it is possible. Because the 80K and 240K have good accuracy in output frequency, synchronization is well possible even by setting a different frequency for them with separable elements.

Q: How can I do for example?

A: Let us assume that synchronous operation (not interpolation) is achieved with a speed ratio of a:b for A and B axis. In the case of constant-speed operation, it is good if the value set on the register is a:b. In the case of accelerated/decelerated operation, set the both axes so that the ramping-up time and the ramping-down time for both axes are equal, in addition to the FL register value of a:b.
If data for both axes are written before the start and the start commands for them are written successively, start difference is due to the CPU's processing time.)



Q: Triangular drive is possible?

A: Yes, it is possible by setting down-point (R6) data to permit triangular drive.
Usually, set so that triangular drive is performed when the number of preset pulses is smaller than the sum of the number of pulses needed for ramping-up and that needed for ramping-down.
The number of pulses (Psu) needed for ramping-up is:

$$Psu = \frac{[(R2)^2 - (R1)^2] \times (R4)}{16384 \times (R7)}$$

The number of pulses needed for ramping-down (Psd) is:

$$Psd = \frac{[(R2)^2 - (R1)^2] \times (R5)}{16384 \times (R7)}$$

Therefore, triangular drive must be performed when

$$(R0) < \frac{[(R2)^2 - (R1)^2] \times [(R4) + (R5)]}{18384 \times (R7)}$$

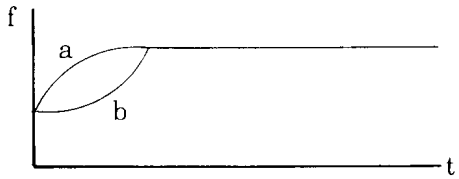
The down-point at that time is:

$$(R6) = (R5)/[(R4) + (R5)] \times (R0)$$

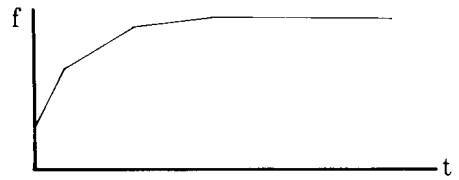
Q: With registered to register R0 ~ R7, unused registers need not be set?

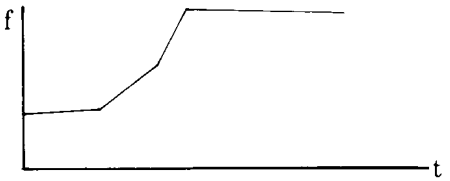
A: The multiplying register does not operate unless it is set. Besides, any data must be set on R1 register.

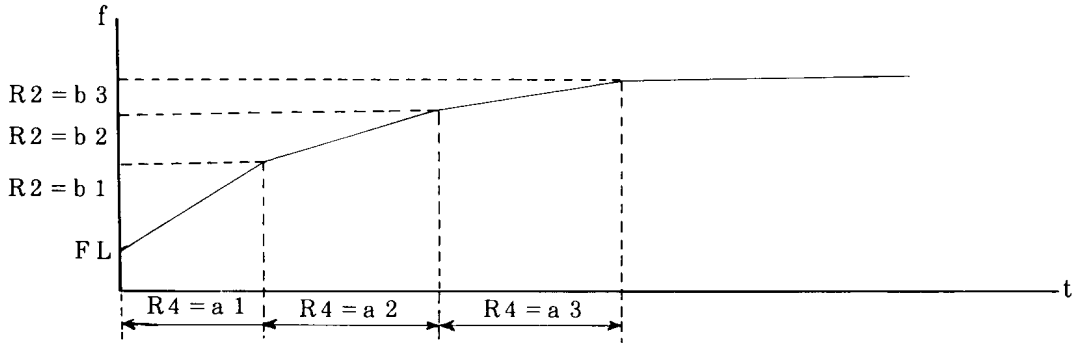
Q: Assuming that the PCL-240K makes linear acceleration, is acceleration possible in any desired curve as shown by (a) and (b), for example? If it isn't possible, is it possible if stepwise?



A: Acceleration such as (a) and (b) is impossible because the PCL-240K permits only linear acceleration and deceleration. If the accelerating time is extremely long, compared with the processing speed of the CPU that controls the PCL-240K, accelerating rate and speed register value successively.

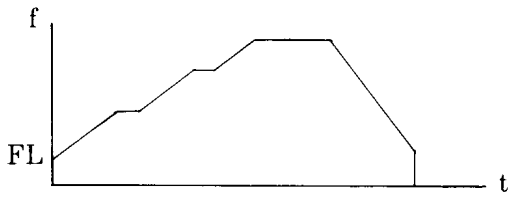






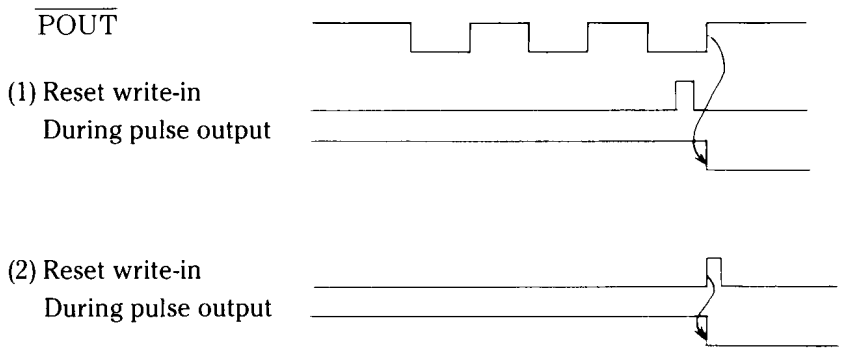
Q: Is it possible to change the speed several times during ramping-up in the perfect ramping-up mode of PCL-240K?

A: It is possible by changing the speed register value successively if the acceleration time is extremely long compared with the processing speed of the CPU that controls the PCL-240K.
At the time of deceleration, however, it decelerate linearity down to FL speed.



Q: Is it possible to change the ramping-down point and stop position during operation in the high-speed preset mode?
A: R0 and R6 should not be changed during operation in the high-speed preset mode, because R0 and R6 have a bit length of 24 bits and 20 bits respectively and the timing of changing the value from CPU is not the same in all bits.

Q: It may sometimes occur that stop is effected by the reset command during operation, but the status in pulse output (bit 6) does not change.
A: During pulse output ("Low" level), the status is set after pulse has been completely outputted.



Q: It may sometimes occur that a low-order digit does not change when counter contents are read during operation.
A: When CPU reads low-order, middle-order and high-order carry-down is effected during this timing difference period, a wrong value may be read. To get the correct value, read high-, middle and low-order bits in this order, then read the middle- and high-order bits again and repeat procedure until the values agree perfectly.

Q: The PCL-240K has many GNDs.
A: Because the speed of the IC itself has become almost twice as fast, we increased GNDs for safety.

Note: Specifications are subject to change without prior notice for improvement.

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